## **MODULAR ARCHITECTURE FOR ROBUST COMPUTATION**

## Session: SpaceWire Onboard Equipment and Software,

## **Short Paper**

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## ABSTRACT

The emergence of the SpaceWire standard as a space data bus is now well established in onboard systems. The related SpaceWire data handling systems are oriented towards SpaceWire network architectures.

This paper presents a Modular Architecture for Robust Computing "MARC" that is a system based on a SpaceWire network architecture targeting missions requiring high reliability and fault-tolerant capabilities as on-board computing systems or extensive processing capabilities, such as advanced payload data processing systems and highly autonomous space exploration systems.

MARC design is based on HW modules sharing HW resource (e.g. communication network, memory, etc.). MARC modularity will allow easy hierarchical scaling of the functional and data flow designs for multi-satellite missions and comprehensive space/ground segment systems. A key feature of MARC is its Active Backplane that determines the network topology. The system implements the latest semiconductor technology developments that have been funded by ESA for space applications, including the LEON2FT fault tolerant processor, SpaceWire and Remote Access Protocol (RMAP) IP Cores and 8 port SpaceWire router.

MARC SW architecture is based on CCSDS SOIS layered model based on a hard real-time operating system using SpaceWire network as a communication means upon which SOIS services can be deployed.

The paper will highlight MARC capabilities as it is envisaged to use it in future ESA missions. The main applications foreseen include missions requiring extensive fault-tolerant on-board computing capabilities, such as advanced platform and payload computing systems and highly autonomous space exploration systems.